Docket No.: S1022.80278US00
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	David Alan Edwards et al.
Serial No.:	09/411,792
Confirmation No.:	8808
Filed:	October 1, 1999
For:	INTERFACE FOR TRANSFERRING DEBUG INFORMATION
Examiner:	Ted T. Vo
Art Unit:	2191

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Dated: October 24, 2008

Amy J. Sendell

REPLY BRIEF

Mail Stop Appeal Brief - Patents
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Dear Sir:

This Reply Brief is submitted in response to the Examiner's Answer dated August 25, 2008. The Examiner's Answer responds to the following arguments made in Appellant's Appeal Brief: (1) Neither of the cited references discloses transmitting an operand address from a processor to a debug circuit; and (2) Neither of these references discloses the use of a single integrated circuit. This Reply Brief is submitted to address the Examiner's comments with respect to each of these arguments, where Appellant believes further discussion would be of use to the Board. Where Appellant has not provided further discussion, Appellant believes the arguments in the Appeal Brief to be sufficient. Appellant continues to maintain all of the arguments presented in the Appeal Brief.

1. **Neither Of The Cited References Discloses Transmitting An Operand Address From A Processor To A Debug Circuit**

The Examiner maintains his contention that MotorolaNPL discloses transmitting an operand address from a processor to a debug circuit. This contention is simply incorrect.

In support of this contention, the Examiner relies on an example from MotorolaNPL shown in Fig. 7 on page 6 (see Examiner's Answer, pages 9-13). This example depicts an illustrative program sequence, showing the instruction address for each instruction in the sequence and the instruction that is stored at each address. Below the program sequence is a code listing showing the information that is transmitted on the DDATA and PST signals during execution of each of the instructions shown in the program sequence.

The Examiner correctly points out that, during execution of the instruction having address 00001318, the DDATA signal transmits the **operand values** for this instruction (see Examiner's Answer, page 12) That is, the fourth line of the code listing in Fig. 7 showing PST/DDATA synchronization indicates that bits 0 to 3 of the write operand for instruction 1318 are transmitted on the DDATA signal, and the fifth line of this code listing indicates that bits 4 to 7 of the write operand are transmitted on the DDATA signal. Appellant emphasizes that the data transmitted by the DDATA signal are **operand values**, not operand addresses. Moreover, as shown in Fig. 3 on page 2 of MotorolaNPL and in Fig. 1 of Circello, the DDATA signal is transmitted from the debug module to an external development system. Thus, even if the information in the DDATA signal is somehow considered to be an operand address (though it clearly is not), any such information is not transmitted from the processor to the debug circuit, but rather is transmitted from the debug circuit to an external development system.

The Examiner appears to contend that the instruction address "00001318" is in the KADDR signal on the K-Bus at the same that the operand values for the instruction stored at this address are on the DDATA bus (*see* Examiner's Answer, page 12). In support of this contention, the Examiner cites a paragraph from page 3 of MotorolaNPL which states, "[t]o capture data and display it on the DDATA port, the WDDATA instruction fetched the operand defined in the effective address, then

place the appropriate number of nibbles on the DDATA output pins, independent of any debug configuration."

Notably, this paragraph does not discuss the KADDR signal or what is being transmitted on the K-Bus when operand values are being transmitted via the DDATA signal. Rather, the cited paragraph is entirely unrelated to the above-discussed example of Fig. 7, and describes a WDDATA instruction, which MotorolaNPL indicates is one of a number of new instructions added to the 68000 family instruction set to accommodate the debug unit (see MotorolaNPL, page 3). The cited paragraph states that the WDDATA instruction places operand values on the DDATA output pins, but does not say anything about the KADDR signal or the K-Bus, and is entirely unrelated to the example shown in Fig. 7. As such, the Examiner's contention that the instruction address "00001318" is in the KADDR signal on the K-Bus at the same that the operand values for the instruction stored at this address are on the DDATA bus is entirely unsupported.

Moreover, the Examiner appears to contend that because the instruction address "00001318" is purportedly in the KADDR signal on the K-Bus at the same time that the operand values for the instruction at this address are in the DDATA signal (though this is clearly not the case), the instruction address "00001318" somehow serves as an operand address for these operand values. This analysis is incorrect.

Even if it is assumed that the instruction address is in the KADDR signal at the same time that the operand values for this instruction are in the DDATA signal (which is not disclosed or suggested by either reference), the instruction address does not identify the memory location at which the operand values are stored, and therefore cannot be considered an operand address. Rather, the instruction address identifies the memory location at which the instruction is stored, not the memory locations at which the operands are stored. Indeed, the memory location at which the operands are stored are specified by the instruction. That is, the operand addresses are included in the instruction, but are not transferred from the processor to the debug module.

2. **Neither Reference Discloses The Use Of A Single Integrated Circuit**

In Appellant's Appeal Brief, Appellant noted that independent claim 21 is directed to a microcomputer implemented on a single integrated circuit. On page 13, of the Examiner's Answer, the Examiner appears to concede that neither Circello nor MotorolaNPL discloses that the components recited in claim 1 (i.e., at least one processor, a debug circuit, a system bus, and a communication link) are implemented on a single integrated circuit, but contends that the system described in Circello and MotorolaNPL functionally acts as a single integrated circuit.

Even if it is assumed that that the system disclosed in Circello and MotorolaNPL performs the same functionality as the system recited in claim 21 (which Apellant does not concede), the microprocessor recited in claim 21 is structurally different from the system disclosed in Circello and MotorolaNPL because it requires that the components of the mircroprocessor listed in the claim be implemented on a single integrated circuit. Because claim 21 is directed to an apparatus (i.e., a microprocessor), and the claimed apparatus is structurally different from the system described in the prior art references, claim 21 patentably distinguishes over the cited references.

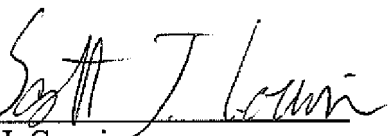
The Examiner also appears to contend that the limitation of claim 21 that requires that the microcomputer be implemented on a single integrated circuit should not be given patentable weight because it appears in the preamble. This is simply incorrect. MPEP §2111.02(I) states, "[a]ny terminology in the preamble that limits the structure of the claimed invention **must** be treated as a claim limitation (emphasis added)." Here, the limitation of claim 21 that requires that the microcomputer be implemented on a single integrated circuit is a structural limitation that defines physical characteristics of the microcomputer. Thus, this limitation must be given patentable weight.

CONCLUSION

Because the pending claims patentably distinguish over the applied references, a sustainable rejection under 35 U.S.C. §102 has not been set forth. Accordingly, the rejection of those claims under 35 U.S.C. §102 should be reversed.

Dated: October 24, 2008

Respectfully submitted,

By 

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